What is claimed is:

1. A packaging structure for back-to-back chips, including:

a substrate;

a first chip, having an active side and an inactive side, and the active side of the first chip partially combining with the substrate and conducted with the substrate by wire-bonding;

a second chip, having an active side and an inactive side, and the inactive side of the second chip combining with the inactive side of the first chip, while the active side of the second chip conducted with the substrate by wire-bonding; and

an encapsulation, covering the first chip and the second chip for protecting the packaging structure for back-to-back chips.

2. The packaging structure for back-to-back chips as recited in claim 1, wherein the combination between the first chip and the substrate is made by the adhesion manner of an adhesion layer.

3. The packaging structure for back-to-back chips as recited in claim 1, wherein the combination between the second chip and the first chip is made by the adhesion manner of an adhesion layer.

4. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with same size.

5. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with different size.

6. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with same function.

7. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with different function.

8. The packaging structure for back-to-back chips as recited in claim 1, wherein arranged plural solder balls are on the substrate and the packaging structure for back-to-back chips is coupled with a circuit board by the solder

balls.

9. A packaging process for back-to-back chips as claim 1, comprising following steps:

a) providing a first chip, a second chip and a substrate, wherein the first chip and the second chip having an active side and an inactive side respectively;

b) combining the active side of the first chip partially with the substrate;

c) conducting the active side of the first chip to the substrate by wire-bonding;

d) combining the inactive side of the second chip with the inactive side of the first chip;

e) conducting the active side of the second chip to the substrate by wire-bonding.

10. The packaging process for back-to-back chips as recited in claim 9, wherein, after the "step e", several steps are further included as follows:

f) covering the first chip and the second chip by an encapsulation for protecting the packaging structure for back-to-back chips;

g) arranging plural solder balls on the substrate for coupling other circuit board by said solder balls.

11. The packaging process for back-to-back chips as recited in claim 9, wherein the combination between the first chip and the substrate is made by the adhesion manner of an adhesion layer.

12. The packaging process for back-to-back chips as recited in claim 9, wherein the combination between the second chip and the first chip is made by the adhesion manner of an adhesion layer.

13. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with same size.

14. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with different size.

15. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with same function.

16. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with different function.